some of the unimplanted epitaxial silicon remains below the respective source or drain region. The metallization includes metal lines which are all located above the epitaxial silicon layer 14. Contact pads are then formed on the integrated circuits 16A and 16B. The integrated circuits 16A and 16B are identical to one another and are separated from one another by a small scribe street 18. Bumps 20 are then formed on the contact pads on the integrated circuits 16A and 16B. Although not shown, the bumps 20 are in an array and rows and columns on a respective integrated circuit 16A and 16B. --

IN THE CLAIMS

Please cancel claims 3, 6, 18-24, and 28-30 without prejudice. Please amend the following claims which are pending in the present application:

1. (Amended) A wafer comprising:

a layer of solid diamond;

a layer of monocrystalline semiconductor material in direct contact with the layer of solid diamond; and

a plurality of integrated circuits formed on the layer of monocrystalline semiconductor material.

2. The wafer of claim 1 wherein the layer of solid diamond is at least 200 mm wide.

4. (Amended) The wafer of claim 1 wherein the layer of monocrystalline

semiconductor material is at least 200 mm wide.

5. (Amended) The wafer of claim 1 wherein the layer of monocrystalline semiconductor material is a layer of monocrystalline silicon.

7. The wafer of claim 1 further comprising:

a plurality of contacts on the integrated circuit.

8. (Amended) A wafer comprising:

a layer of solid diamond;

a final monocrystalline semiconductor film on the layer of solid diamond; and

a layer of monocrystalline semiconductor material directly on the final monocrystalline semiconductor film with a boundary defined between the final monocrystalline semiconductor film and the layer of monocrystalline semiconductor material for purposes of shearing the layer of monocrystalline semiconductor material from the final monocrystalline semiconductor film.

9. The wafer of claim 8 wherein the layer of solid diamond is at least 200 mm wide.

10. The wafer of claim 9 wherein the layer of monocrystalline semiconductor material is at least 200 mm wide.

11. The wafer of claim 10 wherein the layer of monocrystalline semiconductor material is a layer of monocrystalline silicon.

12. (Amended) A singulated die comprising:

a layer of solid diamond having an exposed lower surface; and

an integrated circuit on the layer of solid diamond.

13. (Amended) The singulated die of claim 12 further comprising:

a layer of monocrystalline semiconductor material on the layer of solid diamond, the integrated circuit being formed on the layer of monocrystalline semiconductor material.

14. The singulated die of claim 13 wherein the layer of monocrystalline semiconductor material is a layer of monocrystalline silicon.

15. The singulated die of claim 14 further comprising:

a layer of polysilicon on the layer of monocrystalline silicon, the layer of monocrystalline silicon being located on the layer of polysilicon.

16. The singulated die of claim 12 further comprising:

a plurality of contacts on the integrated circuit.

17. (Amended) The singulated die of claim 12 wherein the die has a rectangular outline when viewed from above.

25. (Amended) A wafer, comprising:

a layer of solid diamond having a thickness ~~of~~ less than 150 microns; and

a plurality of integrated circuits in rows and columns on the layer of solid diamond.

26. ~~(Amended)~~ The wafer of claim 25 further comprising:

a layer of monocrystalline semiconductor material between the layer of diamond and the integrated circuit.

27. (Amended) The wafer of claim 26 wherein a layer of ~~monocrystalline~~ semiconductor material is a layer of silicon.

REMARKS

Claim Objections

Applicant has made the necessary changes to overcome the Examiner's objections to the claims. The word "moncrystalline" has been changed to "monocrystalline."

35 U.S.C. § 112 Rejections

The Examiner has rejected claims 19, 24, and 27 under 35 U.S.C. § 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which Applicant regards as the invention. Claims 19 and 24 have been deleted. Claim 27 has been amended to be in line with the Examiner's assumption that "polysilicon" is to be "silicon."

Applicant, accordingly, respectfully requests withdrawal of the rejections of claims 19, 24, and 27 under 35 U.S.C. § 112, second paragraph.

35 U.S.C. § 102 Rejections

The Examiner has rejected claims 1, 2, and 12 under 35 U.S.C. § 102(b) as being anticipated by Liu. Applicant submits that these claims, as amended, are not anticipated by Liu.

Claim 1 now includes the limitation that a layer of monocrystalline semiconductor material is in direct contact with the layer of solid diamond, and that the integrated circuits are formed on the monocrystalline semiconductor

material. Support for claim 1 as amended can, for example, be found in Figure 1a and accompanying description.

Applicant believes that the Schrantz reference cited by the Examiner is more relevant with respect to claim 1 than Liu. Applicant submits that Liu does not disclose the limitations of claim 1, even without the amendments. Liu does disclose that diamond can be used as a thermal heat sink, for example on Page 1, Lines 1-4; Table 1, Line 6; and Page 3, second to last line. However, Liu does not disclose that diamond can be formed in wafer form with a plurality of integrated circuits on the diamond. Reference is made in Liu to diamond as a semiconductor, for example on Page 1, Line 2, but not on a semiconductor. Reference is also made to growing of diamond on various substrates of various sizes, in particular on Pages 5 to 6, but no reference is made to growing of diamond on semiconductor wafers. As can be seen from Table 2, there is no specific example of the use of diamond on a semiconductor wafer.

As such, Applicant believes that claim 1 is not anticipated by Liu.

As mentioned, Applicant believes that Schrantz is more relevant with respect to claim 1. With specific reference to Figure 1E of Schrantz, it can be seen that a monocrystalline device quality layer 30 is formed on a layer of diamond 12. However, the layer 30 is not in direct contact with the layer of diamond 12, which is a limitation of claim 1 as amended. Neither is there any suggestion in Schrantz or any other reference cited by the Examiner to form a layer of monocrystalline semiconductor material in direct contact with a layer of solid diamond.

Claim 2 depends from claim 1, and should be allowable for the same reasons as claim 1.

With respect to claim 12, Applicant similarly submits that Liu is not relevant to claim 12 before amendment, because Liu does not teach or suggest the use of a layer of solid diamond together with an integrated circuit, as claimed. With reference to Schrantz, it can be seen that the layer of diamond 12 is covered with a die attach layer 22, and therefore does not have any exposed lower surface. There is no suggestion in Schrantz that the die attach layer 22 can be removed.

Applicant, accordingly, respectfully submits that claims 1, 2, and 12 are not anticipated by Liu or by Schrantz.

The Examiner also rejected claim 8 under 35 U.S.C. § 102(b) as being anticipated by Schrantz. Applicant submits that claim 8, as amended, is not anticipated by Schrantz.

Claim 8, as amended, includes a layer of solid diamond, a final monocrystalline semiconductor film, and a layer of monocrystalline semiconductor material, respectively represented by reference numerals 52, 56B, and 56A in the exemplary Figure 2e.

Claim 8 also includes the limitation that a boundary is defined between the final monocrystalline semiconductor film and the layer of monocrystalline semiconductor material for purposes of shearing the layer of monocrystalline semiconductor material from the final monocrystalline semiconductor film. The boundary is indicated with reference numeral 60 in Figure 2e. As illustrated in

0Figure 2h, the boundary serves as the plane where the monocrystalline silicon wafer 56A shears from the final monocrystalline silicon film 56B.

Schrantz does not disclose the boundary as claimed. Neither does Schrantz or any other reference teach or suggest that such a barrier would be required.

Applicant, accordingly, respectfully submits that claim 8 is not anticipated or suggested by Schrantz.

The Examiner also rejected claims 18-19 and 23-25 under 35 U.S.C. § 102(b) as being anticipated by Nagy. Only claim 25 remains pending. Applicant submits that claim 25, as amended is not anticipated by Nagy.

Claim 25, as amended, includes the limitation that the layer of solid diamond is a thin layer, having a thickness of less than 150 microns. Support for the amendment can be found in Figures 2a, 2b, and 2e-j and accompanying description. It is possible to grow the thin diamond layer 72 because of the additional support provided by the sacrificial polysilicon wafer 70. What should be noted is that claim 25 includes the limitation of a plurality of integrated circuits formed on the layer of solid diamond, i.e., at wafer level.

Nagy discloses a package-level device, wherein only a single integrated, in the die 11, is located on the diamond substrate 20. There is no suggestion in Nagy of a plurality of integrated circuits in rows and columns on a layer of solid diamond.

As such, Applicant respectfully submits that claim 25 is not anticipated by Nagy.